In the Specification

Please amend the specification of this application as follows:

LC 11/17/06

Rewrite the paragraph at page 3, lines 3 to 13 as follows:

--Traditionally, critical I/O timing specifications make it necessary for designers to comprehend all of the following design ~~characteristics"(a)~~ characteristics: (a) I/O interface design/architecture; (b) simplified clock distribution; (c) master/slave protocols; (d) self-clocking techniques including the use of analog or digital phase locked loop functions to create alignments between I/O circuit ~~&~~ and process; (e) I/O buffers designed for low voltage-temperature performance variation; (f) rigid process controls; (g) I/O test screening; and (h) speed sort parts by I/O speeds/application. All these design and application considerations involve sophisticated design/process practices and/or compromises in design/process.--

Rewrite the paragraph at page 5, lines 11 to 19 as follows:

--In the program mode, incoming PData In 107 is latched into the PData flip-flop 102 and programmed into the eFuse element on the occurrence of one or more program pulses initiated at Program input 110. PData Out passes to the next eFuse cell via path 116. In the program mode PData Out is passed through multiplexers 104 and 105 and is latched into the CData flip-flop ~~102~~ 103. The voltage VPP 109 is the programming power source. Program data is passed serially to the next cell in the chain at PData Out line 116.--

Rewrite the paragraph at page 10, lines 5 to 24 as follows:

--Figure 3 illustrates a high-speed I/O buffer block 300 for a processor device with boundary 303 showing the associated input and output register stages and pertinent signal and specification definitions. System clock 310 ~~is~~ passes to input and output